a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input of the output stage.

21. (AMENDED) The data transfer arrangement in accordance with claim 1 wherein the bus drivers comprise active pull-up and active pull-down bus drivers.

34. (NEW) The data transfer arrangement in accordance with claim 1, wherein the first stage of the latching sense amplifier comprises:

a plurality of input pass transistors each having a gate, a source terminal, and a drain; and

a plurality of NMOS and PMOS transistors each having a gate, a source terminal, and a drain;

wherein the drains of the input pass transistors are coupled to the drains of the cross-coupled latch amplifier NMOS and PMOS transistors, each source terminal of the input pass transistors is coupled to an input, the sources of the cross-coupled latch amplifier NMOS transistors are coupled to the drain of the NMOS transistor coupled to a clock signal input, and the sources of the PMOS transistors are coupled to the drain of the PMOS transistor having a gate coupled to an inverted clock signal input.

35. (NEW) The data transfer arrangement in accordance with claim 1, wherein the output stage of the latching sense amplifier comprises:

a plurality of input transistors each having a gate, a source terminal, and a drain; and

a pair of cross-coupled PMOS transistors each having a gate, a source terminal, and a drain;

a first PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of the first of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the first of the input transistors; and

a second PMOS transistor having a gate, a source terminal, and a drain, the gate being coupled to a clock signal input; the source being coupled to the source of a second of the cross-coupled PMOS transistors; and the drain being coupled to the drain of the second of the input transistors;

wherein the sources of the input transistors are coupled to a source of an NMOS transistor having a gate coupled to a clock signal input;

wherein the sources of the cross-coupled PMOS transistors are coupled to a voltage supply, the drains of the cross-coupled PMOS transistors are coupled to the drains of the input transistors; and

wherein the drains of the cross-coupled transistors provide a true and a complement phase of a data output signal.

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5 6. (NEW) The data transfer arrangement in accordance with claim 1, wherein the voltage precharge source is configured to precharge the differential bus to a predetermined voltage that is less than a logic high voltage and greater than a logic low voltage.

6 7. (NEW) The data transfer arrangement in accordance with claim 1 further comprising a precharge circuit coupled between the precharge source and the differential bus.

7 8. (NEW) The data transfer arrangement in accordance with claim 3 wherein the active pull up and pull down bus drivers are NMOS transistors.

8 9. (NEW) A method of operation of a data transfer arrangement comprising:

two bus drivers;

a voltage precharge source;

a differential bus coupled to the bus drivers and to the voltage precharge source; and

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a latching sense amplifier coupled to the differential bus;

wherein the latching sense amplifier comprises:

a first stage including a cross-coupled latch coupled to a differential data bus; and

an output stage coupled to an output of said first stage;

wherein the output of the first stage is coupled to an input, and

wherein the sense amplifier operates in two phases:

a precharge phase and a data transfer phase;

wherein the precharge phase operates when a control input clock signal is low, said phase comprising the steps of:

isolating the cross-coupled latch amplifier from a plurality of power buses by turning off an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to the inverted clock signal input;

passing a bus voltage swing to a plurality of internal nodes IT and IC of the latched amplifier;

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precharging both dynamic gates to Vdd; and

providing a high true phase and a high complement phase of a data output signal; and

wherein the data transfer phase operates when a control input clock signal is high, said phase comprising the steps of:

isolating the internal nodes of the latched amplifier from the bus lines by turning off the pass input transistors;

connecting the cross-coupled latched amplifier to power buses by turning on an NMOS transistor coupled to the clock signal input and a PMOS transistor coupled to an inverted clock signal input;

amplifying each low voltage swing of the internal nodes to full logic levels;

discharging an output node of one of the dynamic gates to ground; and

providing a low true phase and a low complement phase of the data output signal.